CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 16, 2003.

Attorney for Applicant(s)

PATENT APPLICATION
Docket No.: END920020059US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	David Alan Burton and Noel Simen Otterness	)
		)
Serial No.:	Not yet assigned	)
		) Group Art
Filing Date:	December 16, 2003	) Unit:
		)
For:	APPARATUS METHOD AND SYSTEM FOR FAULT TOLERANT MEMORY MANAGEMENT	)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Information Disclosure Statement discloses information which has come to the attention of applicant and his attorneys and is being submitted so as to comply with the duty of disclosure set forth in 37 C.F.R. § 1.56. In accordance with 37 C.F.R. § 1.97(b), this Statement is being filed within three (3) months of the filing date of the above-identified application or before the mailing date of a first Action on the merits.

Neither applicant nor his attorneys make any representation that any information disclosed herein may be "prior art" within the meaning of that term under 35 U.S.C. §§ 102 or 103. Moreover, pursuant to 37 C.F.R. § 1.97, the filing of this Information Disclosure Statement

shall not be construed as a representation that a search has been made or as an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

In accordance with 37 C.F.R. § 1.98, this Information Disclosure Statement includes and is accompanied by:

1. A completed copy of Form PTO-1449 listing the patents, publications and other information being submitted for consideration; and
2. A legible copy of each publication and other item of information in written form listed on the enclosed Form PTO-1449.

NON-ENGLISH INFORMATION

Pursuant to 37 C.F.R. § 1.98, following is a concise explanation of the relevance (as it is presently understood by the individual designated in 37 C.F.R. § 1.56(c) most knowledgeable about the content of the information), of each listed patent, publication or other information that is not in the English language.

JP7013789A
Abstract

Problem To Be Solved: To provide an automatic and prompt method to recover from a small step-out event.
Solution: A ***memory*** ***management*** system for a ***fault*** ***tolerant*** computer system includes a first recording mechanism 25 capable of recording the ***memory*** updating (writing) event, a second recording mechanism 26 provided with capacity to record the ***memory*** updating event, a fault input for a fault signal to activate the first recording mechanism in the case of the fault (step-out) event and a ***memory*** reintegration mechanism 27 at least to reintegrate the ***memory*** of the part which discriminated by the first and the second recording mechanisms. Since only comparatively small number of locations are corrected in both ***memory*** systems of processing sets of step-out and in operation, recovery from the small step0out between the processing sets in a system of lock-step method is promptly

and effectively achieved by copying a ***memory*** page discriminated by the first and the second recording mechanisms from the processing set in operation to the step-out processing set.

JP2202637A

Abstract

A computer system in a fault-tolerant configuration employs three identical CPUs executing the same instruction stream, with two identical, self-checking memory modules storing duplicates of the same data. Memory references by the three CPUs are made by three separate busses connected to three separate ports of each of the two memory modules. The three CPUs are loosely synchronized, as by detecting events such as memory references and stalling any CPU ahead of others until all executed the function simultaneously; interrupts can be synchronized by ensuring that all three CPUs implement the interrupt at the same point in their instruction stream. Memory references via the separate CPU-to-memory busses are voted at the three separate ports of each of the memory modules. I/O functions are implemented using two identical I/O busses, each of which is separately coupled to only one of the memory modules. A number of I/O processors are coupled to both I/O busses. Each CPU has it own fast cache and also local memory not accessible by the other CPUs. A hierarchical virtual memory management arrangement for this system employs demand paging to keep the most-used data in the local memory, page-swapping with the global memory. Page swapping with disk memory is through the global memory; the global memory is used as a disk buffer and also to hold pages likely to be needed for loading to local memory. The operating system kernel is kept in local memory. A private-write area is included in the shared memory space in the memory modules to allow functions such as software voting of state information unique to CPUs. All CPUs write state information to their private-write area, then all CPUs read all the private-write areas for functions such as detecting differences in interrupt cause or the like.

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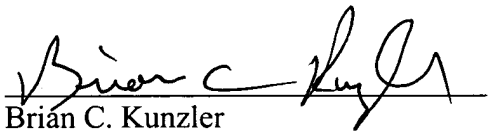
Respectfully submitted,



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FORM PTO-1449 **LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT** (use several sheets if necessary)	SERIAL NO. Not yet assigned	ATTORNEY DOCKET NO. END920020059US1
	FILING DATE December 16, 2003	GROUP ART UNIT
	APPLICANT(S): David Alan Burton and Noel Simen Otterness	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
	A1	4,187,554	02/05/1980	Kammann	365/15	04/24/1978
	A2	4,942,579	07/17/1990	Goodlander et al.	371/51	02/27/1989
	A3	5,299,202	03/29/1994	Vaillancourt	371/11.1	12/07/1990
	A4	5,325,517	06/28/1994	Baker et al.	395/575	05/17/1989
	A5	5,537,631	07/16/1996	Wong et al.	395/182.05	03/21/1994
	A6	5,553,263	09/03/1996	Kalish et al.	395/454	07/16/1993
	A7	5,708,771	01/13/1998	Brant et al.	395/182.2	11/21/1995
	A8	5,784,548	07/21/1998	Liong et al.	395/182.04	03/08/1996
	A9	5,887,270	03/23/1999	Brant et al.	711/162	09/22/1997
	A10	5,896,492	04/20/1999	Chong, Jr.	395/182.01	10/28/1996
	A11	5,953,742	09/14/1999	Williams	711/154	07/01/1996
	A12	5,991,852	11/23/1999	Bagley	711/112	10/28/1996
	A13	6,065,102	05/16/2000	Peters et al.	711/151	11/07/1997
	A14	6,105,116	08/15/2000	Mori	711/162	12/23/1997
	A15	6,295,594	09/25/2001	Meier	711/171	02/17/2000

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION	
						YES	NO
	A16	10 177 498	06/30/1998	JP	GO6F11/18		X

EXAMINER	**DATE CONSIDERED**

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

	A17	2 202 637	06/13/1990	JP	GO6F11/16		X
	A18	7 013 789	06/13/1990	JP	GO6F11/16		X
	A19	0 817 053	01/07/1998	EP	GO6F11/18	X	
	A20	0 372 578	06/13/1990	EP	GO6F11/16	X	

NON-PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT (Including Author, Title, Source, and Pertinent Pages
	A21	Nicholas S. Bowen, et al. "A Fault Tolerant Hybrid Memory Structure and Memory Management Algorithms", IEEE Transaction on Computers, Vol. 44 No. 3, March 1995.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).